Fast Capacitance Extraction of Actual 3-D VLSI Interconnects Using Quasi-Multiple Medium Accelerated BEM

Wenjian Yu, *Student Member, IEEE*, Zeyi Wang, *Member, IEEE*, and Jiangchun Gu

***Abstract*—In this paper, a quasi-multiple medium (QMM) method based on the direct boundary element method (BEM) is presented to extract the capacitance of three-dimensional (3-D) very large scale integration interconnects with multiple dielectrics. QMM decomposes each dielectric layer into a few fictitious medium blocks, and generates an overall coefficient matrix with high sparsity. With the storage technique of a sparse blocked matrix and iterative equation solver generalized minimal residual, the QMM can greatly reduce the CPU time and memory usage of large-scale direct BEM computation. Numerical examples of 3-D multilayered and multiconductor structures cut from actual layout show the efficiency of the QMM method for capacitance extraction. We also compared the QMM accelerated BEM with geometry independent measured equation of invariance (GIMEI) and Zhu's overlapping domain decomposition method (ODDM). The results show that the CPU time consumed by the above-mentioned methods is on the same order, and the QMM method is superior to the others for fairly large and complex structures. While in memory usage, the QMM accelerated BEM is superior to GIMEI, but inferior to ODDM.**

***Index Terms*—Capacitance extraction, direct boundary element method (BEM), quasi-multiple medium (QMM) method, three-dimensional (3-D) very large scale integration (VLSI) interconnects.**

I. Introduction

In VERY LARGE scale integration (VLSI) circuits, with rapid increase of device density and working frequency, the electrical characteristics of interconnects are becoming more important factors governing the circuit performances such as delay, power consumption, reliability, etc. This has increased the interest in efficient methods for calculating electrical parameters of interconnects.

Since the mid-1990s, many efficient numerical methods have been proposed to calculate the capacitance matrix of interconnects [1]–[11], [18]. They can be classified as the indirect boundary element method (BEM) [1]–[4], direct BEM [5], [6], the method of the measured equation of invariance (MEI) [7], [8], [18], and several kinds of semianalytical approaches [9]–[11]. In both the indirect and direct BEM, only surfaces of three-dimensional (3-D) objects are discretized, and a smaller system of linear equations is obtained. The MEI technique can terminate the meshes very close to the object boundary and still preserves the sparsity of the finite-difference (FD) equations. The geometry independent measured equation of invariance (GIMEI) is proposed for the capacitance extraction of the general two-dimensional (2-D) and 3-D interconnects by using free-space Green's function only [8]. The MEI method has now been developed to on-surface level, where a surface mesh is used to keep the number of unknowns in minimum [18]. The semianalytical approaches usually decompose the simulated region into subregions and analyze them separately. Many subregions with simple geometry can be analyzed analytically, thus, the domains that have to be analyzed numerically are reduced to the least. This dramatically reduces memory and computing time [10]. The overlapping domain decomposition method (ODDM) in [10] is one of these approaches with high performance. In addition, many extraction tools such as Avant!'s Raphael, Ansoft's SpiceLink, and the Massachusetts Institute of Technology's (MIT's) FastCap have been available in practical use.

An interconnect capacitor, which exists in reality, is defined in a finite region and described by the Laplace equation with the mixed boundary conditions [2]. It means that the finite Neumann boundary should be considered. In fact, several published algorithms are all based on the capacitor model with finite Neumann boundaries [2], [5], [9]–[11]. For this capacitor model, the direct BEM is more suitable to extract the capacitance matrix than the indirect BEM. This is because there are two variables of electrical potential and its normal derivative in the direct boundary integral equation (BIE) [12], [13]. Compared with the semianalytical approaches proposed by Hong *et al.* [9] and Zhu *et al.* [10], [11], the direct BEM can deal with more complicated 3-D structure of the interconnects. In fact, the geometry that the semianalytical approaches can deal with has some limitations [8]. However, the direct BEM generally leads to a nonsymmetric coefficient matrix and the matrix for a single dielectric region is dense. This causes a great deal of time and memory consumption in forming and solving the system of linear equations [13].

In this paper, a new quasi-multiple medium (QMM) method is proposed to accelerate the direct BEM computation. It utilizes the localization character of the direct BEM to transfer the coefficient matrix into a highly sparse block matrix. With the technology of storing a sparse block matrix and the iterative equation solver, the QMM method can greatly reduce the CPU time and memory usage of large-scale direct BEM computation. We have

Manuscript received July 10, 2001; revised January 29, 2001. This work was supported by the China National Science Foundation under Grant 69876024 and by the China National Foundation for Key Basic Research under Grant G1998030404. This work was supported in part by Synopsys Inc.

W. Yu and Z. Wang are with the Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China (e-mail: ywj77@computer.org).

J. Gu was with the Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China. He is now with the Huawei Technologies Company Ltd., Shenzhen 518129, China (e-mail: gujc@huawei.com).

Digital Object Identifier 10.1109/TMTT.2002.806923

applied the QMM accelerated BEM to actual 3-D interconnect capacitance extraction. Numerical experiments of 3-D extraction are designed to demonstrate the computational efficiency of our method. The results are in close agreement with those of SpiceLink, FastCap, or Raphael, but the computing time and memory size used by our method are at least ten times less than those used by them. We also compared a QMM accelerated BEM with the ODDM in [10] and GIMEI in [8]. The results show that our method is superior to them in CPU time, especially for fairly large and complex structures. While in memory usage, the QMM accelerated BEM is superior to the GIMEI, but inferior to the ODDM.

The remainder of this paper is organized as follows. Section II outlines the direct BEM and related formulas to calculate interconnect capacitance. The principle of the QMM method is presented in Section III. In Section IV, some important aspects of the QMM accelerated BEM are discussed for actual 3-D capacitance extraction. The numerical results are presented in Section V. Finally, we give conclusions in Section VI.

II. Direct BEM for Capacitance Extraction with Multiple Dielectrics

A. Fundamental Formulation

For an interconnect capacitor with N_c conductors embedded in M dielectric layers, an approach, setting the jth conductor to 1 V and the rest to 0 V, is used to determine the self and coupling capacitances of the jth conductor. This procedure can be repeated N_c times to get the capacitance matrix [2]. In a setting of bias voltages, the conductor of 1 V is called the master conductor, and the others are called the environment conductors.

Within the 3-D domain of the ith dielectric denoted by Ω_i, the electrical potential u is governed by the Laplace equation with mixed boundary conditions

$$\begin{cases} \nabla^2 u = \dfrac{\partial^2 u}{\partial x^2} + \dfrac{\partial^2 u}{\partial y^2} + \dfrac{\partial^2 u}{\partial z^2} = 0, & \text{in } \Omega_i \; i = 1, \ldots, M \\ u = u_0, & \text{in } \Gamma_u \\ q = \dfrac{\partial u}{\partial \boldsymbol{n}} = 0, & \text{on } \Gamma_q \end{cases} \tag{1}$$

where Γ_u is the Dirichlet boundary (surfaces of conductors), where u is known and determined by the bias voltage, and Γ_q is the Neumann boundary (outer surfaces of dielectrics), where the normal electrical field intensity q is supposed to be zero. $\boldsymbol{n}$ stands for the unit vector outward normal to the boundary.

Besides, u and q fulfill the compatibility equations along the interface of two adjacent dielectrics a and b as follows:

$$\begin{cases} \varepsilon_a \cdot \partial u_a / \partial \boldsymbol{n}_a = -\varepsilon_b \cdot \partial u_b / \partial \boldsymbol{n}_b \\ u_a = u_b \end{cases} \tag{2}$$

where ε_a and ε_b stand for the permittivities of dielectric a and b. With the fundamental solution u^* as the weighting function, the Laplace equations in (1) are transformed into following direct BIEs by the Green's formula [13]

$$c_s u_s + \int_{\partial\Omega_i} q^* u d\Gamma = \int_{\partial\Omega_i} u^* q d\Gamma, \qquad i = 1, \ldots, M \tag{3}$$

where u_s is the electrical potential at source point s, c_s is a constant dependent on the boundary geometry near to the point s, and q^* is the derivative of u^* along the outward normal direction of boundary $\partial\Omega_i$.

Employing constant quadrilateral elements and evaluating the direct BIE at collocation points, one for an element, the discretized BIEs for the ith dielectric are obtained as follows:

$$c_k u_k + \sum_{j=1}^{N_i} \left(\int_{\Gamma_j} q^*_{(k)} d\Gamma \right) u_j = \sum_{j=1}^{N_i} \left(\int_{\Gamma_j} u^*_{(k)} d\Gamma \right) q_j, \qquad k = 1, \ldots, N_i \tag{4}$$

where N_i is the number of the boundary elements in dielectric i, and Γ_j is the jth element.

B. Integration and Equation Solution

The evaluation of integrals in (4) is the most time-consuming part of boundary element algorithms, particularly for 3-D analysis [5], [17]. They can be classified as the singular integrals and nonsingular integrals. When the source point is on the same element where the integral is taken, i.e., $k = j$ in (4), it is singular integral, otherwise it is nonsingular integral. For the singular integral, the analytical integral method adopting local polar coordinates is effective [16]. The Gauss–Legendre integration scheme with adaptive determination of integration points is employed to calculate the nonsingular integral [5], [17]. However, for the nearly singular integrals, when the source point is close to the element where the integral is taken, the order of Gauss–Legendre integration is still very high. Thus, reducing the calculating time of the nearly singular integrals becomes very important for direct BEM computation.

We proposed a semianalytical method to deal with these nearly singular integrals. With application of the primitive function, the 2-D integral taken on a trapezoid element is converted into a one-dimensional Gauss–Legendre integration (see the Appendix). Compared with the 2-D Gauss-Legendre integration, the number of integration points is reduced drastically so that higher computational speed and accuracy are achieved.

After the integration, a matrix equation for each dielectric is generated as follows:

$$\boldsymbol{H}^i \cdot \boldsymbol{u}^i = \boldsymbol{G}^i \cdot \boldsymbol{q}^i, \qquad i = 1, \ldots, M \tag{5}$$

where $\boldsymbol{u}^i$ is the column vector of electrical potential on the boundary of the dielectric i, $\boldsymbol{q}^i$ is the column vector of the normal electrical field intensity, and $\boldsymbol{H}^i$ and $\boldsymbol{G}^i$ are the corresponding coefficient matrixes, respectively. Both vectors of $\boldsymbol{u}^i$ and $\boldsymbol{q}^i$ have an order of N_i.

Matrix equations (5) can be put together utilizing the compatibility equations (2). We then reorganize the equation system, such that all unknown variables are collected in a left-hand side vector, while a corresponding right-hand-side vector is obtained by multiplying matrix entries with the known values of u and q. This gives

$$\boldsymbol{A}\boldsymbol{x} = \boldsymbol{f}. \tag{6}$$

The coefficient matrix $\boldsymbol{A}$ is a large nonsymmetric one for the 3-D problem. The Krylove sub-space iterative methods are efficient to solve them. A preconditioned generalized minimal residual (GMRES) algorithm is used here [14]. After solution of (6), the self-capacitances and coupling capacitances can be

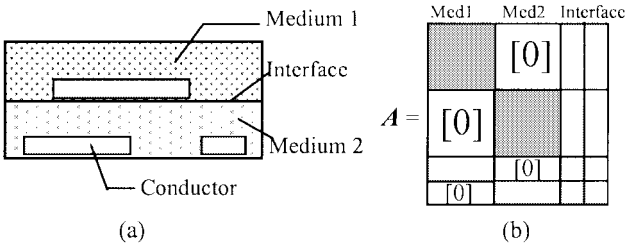


Fig. 1. (a) 2-D problem with two dielectrics. (b) Corresponding coefficient matrix, where the gray blocks denote nonzero entries.

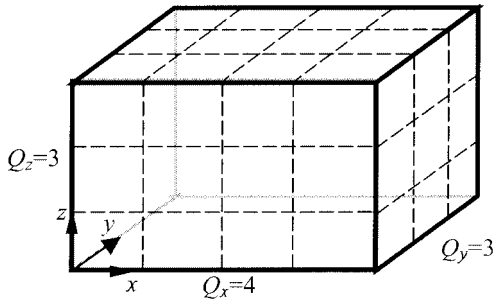


Fig. 2. Single dielectric with a Cartesian coordinate system is cut into $Q = Q_x \times Q_y \times Q_z$ fictitious mediums.

evaluated by the integral of the normal electrical-field intensity on the conductor surfaces [1], [5].

III. Principle of the QMM Method

A. Localization of Direct BEM

From (4), we can see that, in each discretized BIE, all discretized variables are on the boundary elements of one dielectric region. Thus, there are direct interactions among the boundary elements in the same dielectric, which result in nonzero coefficients in the overall equation. We call this the localization character of the direct BEM.

In the linear system (6), the coefficient matrix $\boldsymbol{A}$ reflects the distribution of interactions among all boundary elements. If there is the direct interaction between two elements, nonzero entries are formed by the integrals taken on one of the elements with the source point on the other. Otherwise, when the source point and discrete variable are on the elements without direct interaction, i.e., not involved in a same dielectric, zero entries are formed in the matrix $\boldsymbol{A}$. For a problem with multiple dielectrics, the localization of the direct BEM makes matrix $\boldsymbol{A}$ sparse, from which we could benefit while storing and solving the system of the algebraic equation (6). In Fig. 1, we show a typical capacitor with two dielectrics and the corresponding matrix $\boldsymbol{A}$ generated by the direct BEM, where the nonzero entries and location of discrete variables are indicated.

B. QMM Method

The QMM method takes full advantage of the localization character of the direct BEM. A single dielectric with permittivity ε is regarded as a composition of Q fictitious medium blocks, whose permittivities are all the same as ε, as shown in Fig. 2. Thus, the problem with the single medium is transferred into a problem with some fictitious mediums. Due to the localization character, the dense coefficient matrix for the single medium problem is converted into a sparse one for the problem with multiple mediums.

With suitable decomposition of the single dielectric, the resulting coefficient matrix $\boldsymbol{A}$ will become one with much sparsity so that computational speed-up is available. With the storage technique of the sparse blocked matrix and iterative equation solvers such as the GMRES algorithm, the computing time and memory usage for the original single medium problem will be greatly reduced. We call this the QMM method.

Therefore, the QMM method includes the following three main points. Firstly, a single dielectric is regarded as a composition of some fictitious mediums. Secondly, a suitable strategy of decomposition is considered to make the resulting BEM coefficient matrix with much sparsity. Lastly, the technique of storing the sparse matrix and iterative equation solver are used to benefit from the matrix sparsity.

It should be pointed out that the QMM method adds some unknowns to the overall problem, which are introduced on the additional fictitious interfaces of QMMs. With suitable decomposition of dielectric regions, these unknowns would account for a little percentage of total unknowns since most boundary elements are located on conductor surfaces. Thus, compared with the conventional BEM, the nonzero entries of matrix $\boldsymbol{A}$ are much fewer in the QMM method. Since the Krylove sub-space iterative methods are usually used in 3-D capacitance extraction, fewer nonzero matrix entries mean less memory usage and computing time by using the technique of the storing sparse matrix. Actual cases of 3-D capacitance extraction verified this analysis.

C. Performance Analysis of QMM for Actual Capacitance Extraction

The QMM method has been applied in the extraction of actual 3-D multilayered interconnect capacitance. Here, each dielectric layer is decomposed into a few fictitious medium blocks, the overall coefficient matrix becomes much sparser, and great computational acceleration can be expected. The CPU time and memory usage of QMM for actual capacitance extraction will be analyzed as follows.

The total CPU time used in 3-D interconnect capacitance extraction with the direct BEM can be expressed as follows:

$$t = t_{\text{gen}} + t_{\text{sol}} + t_{\text{aux}} \tag{7}$$

where t_{gen} is the time spent in generation of the coefficients in (6), t_{sol} is the time spent in solution of (6), and t_{aux} stands for the time spent in other supplementary procedures, including input of the structure data and partition of boundary elements. Generally speaking, the sum of t_{gen} and t_{sol} accounts for over 90% of the total CPU time t.

Only nonzero matrix entries need to be computed and stored, thus,

$$t_{\text{gen}} \propto Z \tag{8}$$

where Z stands for the number of nonzero entries of matrix $\boldsymbol{A}$. In the phase of the equation solution, we use the Krylove sub-space iterative methods such as GMRES [14], in which the

main manipulation of each iteration is once matrix–vector multiplication. Thus, we have

$$t_{\rm sol} \propto Z \cdot k \tag{9}$$

where k stands for the number of iterations.

For 3-D capacitance extraction, the coefficient matrix $\boldsymbol{A}$ is usually a nonsymmetric sparse matrix with a large order, e.g., larger than 1000. A good preconditioning matrix should also be selected for the GMRES algorithm to quicken convergence. Properly organizing the discretized BIEs, the diagonal preconditioner can bring quick convergence to the GMRES solver, which will be discussed further in Section IV-D. In this case, the number of iterations k is much less than the parameter Z in (9). Therefore, the number of nonzero matrix entries Z is very significant for the total computing time.

If we ignore the influence of $t_{\rm aux}$ and assume the k does not change much while using the QMM method, we will find out that the fewer nonzero entries there are, the less CPU time will be taken. In formulation, the speed-up ratio of the BEM computation with QMM acceleration is expressed as

$$R_{\rm speed-up} = t/t' \approx Z/Z' \tag{10}$$

where Z and Z' stand for the numbers of nonzero entries of matrix $\boldsymbol{A}$ in the BEM computation without QMM acceleration and that with QMM acceleration, respectively. This expression reveals that the ratio of number of nonzero matrix entries approximately equals to the speed-up ratio of the QMM method. Thus, when the QMM method is applied to actual 3-D capacitance extraction, its efficiency is mainly determined by the reduction of the nonzero matrix entries.

In our implementation of BEM computation, the memory usage consists of two main parts. One is the memory needed to store the coefficient matrix, denoted by $\rm Mem_A$ and the other is used to store the orthogonal basis vectors in the GMRES algorithm, denoted by $\rm Mem_V$. With the technology of storing the sparse matrix, we get

$$\rm Mem_A \propto Z \tag{11}$$

which means that $\rm Mem_A$ is proportional to the number of the nonzero matrix entries. In the GMRES algorithm, a new orthogonal basis vector is constructed in each iterative step. Thus, we have

$$\rm Mem_V \propto V \cdot k \tag{12}$$

where V is the number of all unknowns and k is the number of iterations. Since double precision arithmetic is required for only the work comprising the orthogonalization process [19], we store the matrix $\boldsymbol{A}$ in single precision and the basis vectors in double precision. This storing scheme of mixed precision results in less memory storage than the wholly double precision version, while high computational accuracy is preserved [19].

Using the QMM method, $\rm Mem_A$ is reduced by the same ratio with the reduction of nonzero matrix entries. On the other hand, $\rm Mem_V$ is increased because more unknowns are involved. Usually $\rm Mem_A$ is much larger than $\rm Mem_V$. Thus, if the unknowns are not increased much, the total memory usage will be reduced while using the QMM method. This is verified by actual examples of 3-D capacitance extraction, for which several times of reduction in memory could be found while using the QMM method. It should also be pointed out that the increase of memory usage would be possible in the case with unsuitable QMM decomposition, where too many fictitious interfaces of QMMs caused a great increase of unknowns.

IV. QMM Accelerated BEM for Actual Interconnect Capacitance Extraction

In this section, we firstly give the algorithm description of the QMM accelerated BEM. The strategy for decomposition of dielectric layers and element partition is given later. Lastly, we discuss the organization of discretized BEM equations.

A. Algorithm Description

An interconnect capacitor cut from the real layout usually is a stratified structure, and has many conductors embedded in multiple stratified dielectrics. In order to apply the QMM method to actual 3-D interconnect capacitance extraction, we need to decompose the original dielectric layers into some fictitious medium blocks. We then use the direct BEM to calculate the capacitance with the new multidielectric structure. The major steps of our QMM accelerated algorithm are listed as follows.

Step 1) Read in the data describing a 3-D interconnect capacitor.

Step 2) Set element-partitioning gaps for each boundary surface.

Step 3)

```
For i = 1 to M
  Decompose the ith dielectric into fictitious mediums;
  For j = 1 to ConducterNumberInLayer[i]
    If (the jth conductor intersect additional interfaces of fictitious mediums)
      Decompose conductor j according to the decomposition of dielectric i;
      Set containing relationship of conductor blocks and fictitious medium blocks;
    EndIf
  EndFor
EndFor
```

Step 4) Organize medium blocks and conductors blocks into new object lists.

Step 5) Partition all boundary surfaces of the new multidielectric structure.

Step 6) Calculate integrals in (4) and form (6).

Step 7) Solve (6) with the preconditioned GMRES and output the capacitance results.

B. Decomposition of Dielectrics

In order to decrease the additional efforts brought by the QMM decomposition, we adopt a simple strategy. Since every

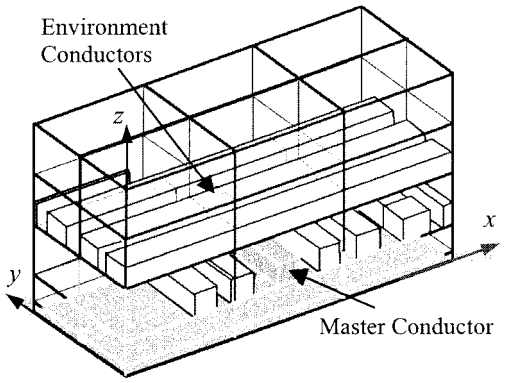


Fig. 3. Typical 3-D interconnect capacitor with five dielectrics is cut into 3 × 2 structures.

dielectric layer is cuboid, and each surface of it parallels to one of the three coordinate planes in the 3-D Cartesian coordinate system, we use two groups of planes parallel to the YOZ- and ZOX-planes, respectively, to cut all dielectric layers into pieces (Fig. 3). Thus, in the top view of the 3-D interconnect capacitor, each original dielectric is decomposed into an array of $m \times n$ fictitious medium blocks. We call (m, n) the QMM cutting number.

The conductor distribution of actual 3-D interconnect capacitor differs in thousands of ways, and the cutting position is not as important as the number Q of fictitious mediums for the QMM's efficiency. Thus, a strategy of proportional-spacing cutting is adopted, i.e., $m-1$ fictitious planes perpendicular to the X-axis and $n-1$ fictitious planes perpendicular to the Y-axis cut the dielectrics uniformly. In Fig. 3, we show a five-layered interconnect capacitor to which a 3×2 QMM cutting is performed.

Now, every dielectric layer is decomposed into $Q = m \times n$ fictitious medium blocks. Neither of little value and great value of Q can bring the best speed-up of QMM computation. Moderate values of m and n should be chosen. Here, an empirical formula is obtained from a great deal of calculation for actual interconnect capacitors according to their dimensions. Finding a way to dynamically determine the optimal QMM cutting number will be explored and discussed in the future.

C. Boundary Element Partition

In applications of the BEM, the partition of boundary elements is very important. It affects both speed and accuracy of BEM computation. In this paper, we adopt a strategy of nonuniform density partitioning. Thus, we partition the boundaries into fewer elements without loss of accuracy.

There are two kinds of boundary surfaces in the actual interconnect structure. Some surfaces can be treated as trapezoid planes without holes, and the other can be treated as planes with some polygon holes. Using the scan-line algorithm, a surface with holes can be further treated as a composition of smaller trapezoids [15]. Hence, both kinds of boundary surfaces consist of the trapezoids, which are called mother elements and need to be further divided into the boundary elements.

According to the electrostatic analysis, the electrical-field intensity on boundary surfaces of conductors, especially the

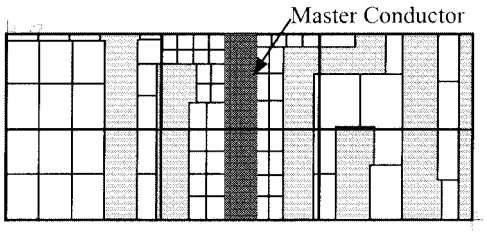


Fig. 4. Boundary element partition of one layer interface in the capacitor shown in Fig. 3.

master conductor, generally is the largest in the simulated region. Besides, the electrical-field intensity at boundary points near the master conductor is also larger. Thus, for each mother element to be partitioned, the mesh number along two directions should be deferent according to its type, position, size, etc. The larger the electrical field intensity on a mother element, the more densely it should be partitioned.

For the additional fictitious surfaces introduced by the QMM, we also use different partition density according to the above electrostatic analysis. For each dielectric layer, the partition density of fictitious surfaces is different. In the dielectric layer containing the master conductor, fictitious surfaces are partitioned more densely. While in the dielectric layers far from the master layer, the partition density can be much less.

In the QMM accelerated BEM, the interface of the dielectric layer is cut into small pieces, and some fictitious surfaces (which may be surfaces with holes) are produced. Thus, the partition of the boundary element becomes more complex than that without QMM accelerating. In Fig. 4, the partition of the bottom surface of the master dielectric layer in Fig. 3 is shown. This complex element partition of nonuniform density brings much difficulty to the more detailed discussion about the influence of the QMM cutting number on computing time.

D. Organization of the Coefficient Matrix

Organization of the coefficient matrix $\boldsymbol{A}$ in multidielectric BEM computation involves the sorting order of unknowns and source points and the storage structure. The order of unknowns determines the arrangement of matrix columns, whereas the order of source points determines the arrangement of matrix rows. We make the order of source points consistent with that of unknowns so that the diagonal entries of the matrix are obtained by the singular integrals. Since the singular integral results in a nonzero entry with larger absolute value, the diagonal preconditioner can bring quick convergence to the GMRES solver.

How to arrange the unknowns or source points, which determines the distribution of nonzero entries in the matrix $\boldsymbol{A}$, is very important for the QMM accelerated BEM. Using the QMM method, the regions of dielectrics are at least several times more than the original structure without fictitious cutting. For example, a three-dielectric capacitor contains 12 dielectric regions, while 2×2 QMM cutting is applied. If the unknowns were arranged without serious consideration, the nonzero entries would disperse in the coefficient matrix. Also, the nonzero matrix blocks would increase much faster than the dielectric regions. This would cause a lot of additional CPU time spent on

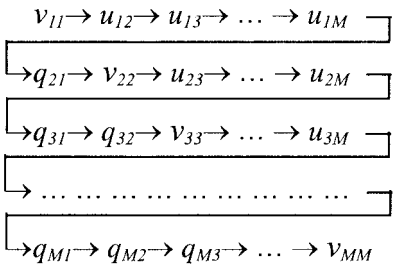


Fig. 5. Matrix expression of the unknown order.

switching manipulation among matrix blocks and locating of nonzero entries in each matrix–vector multiplication. The efficiency of the QMM method would be weakened.

The arrangement of unknowns in the multiregional BEM computation is discussed in [5] and [12] for the direct equation solver. With reference to them, we propose a matrix expression of the unknown order suitable for any complex multiple-medium structure. By this arrangement, the number of nonzero blocks is deceased to the least, and their distribution is so regular that an efficient storage structure can be easily found to save the additional CPU time.

The matrix expression of the unknown order is introduced below. For the ith dielectric region, unknowns in discretized BIEs can be classified into the following three types:

1) u on the Dirichlet boundary and q on the Neumann boundary, denoted by v_{ii};
2) u on the dielectric interface, denoted by u_{ij} (the jth dielectric shares an interface with dielectric i);
3) q on dielectric interface, denoted by q_{ij} (the meaning of j is the same as that in 2).

due to the compatibility of u and q along interfaces [see (2)], u_{ij} and u_{ji} can be represented only by u_{ij} $(i < j)$, while q_{ij} and q_{ji} can be represented by $q_{ij} (i > j)$ $(i > j)$. The order of unknowns follows the rules below, and is expressed by a matrix, as shown in Fig. 5.

1) All possible $M \times M$ types of unknowns are arranged in an $M \times M$ matrix (M is the number of dielectric regions).
2) Entries on the main diagonal are of the type v, while entries in upper triangle are of type u and lower triangle are of type q.
3) The subscript of each matrix entry is the same with its row–column position.
4) From left to right in the first row, and so on, row by row (i.e., follow the arrow lines), we get the order of all unknowns.

Using this order of unknowns and the corresponding order of source points, the coefficient matrix $\boldsymbol{A}$ for the two-dielectric problem in Fig. 1 is shown in Fig. 6(a), where the nonzero entries are distributed more regularly than that in Fig. 1(b). Fig. 6(b) shows the nonzero block distribution for a three-dielectric capacitor applied 2×2 QMM cutting, under our matrix organization. In this case, there are 50 nonzero blocks after merging. While by another arrangement, the number would be 404. It could be proven that our method produces the fewest

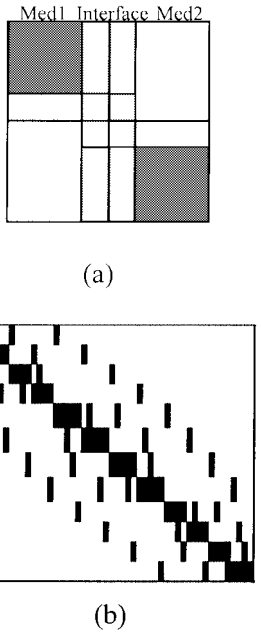


Fig. 6. Distribution of the nonzero matrix entries for: (a) the two-dielectric problem in Fig. 1 and (b) a three-dielectric capacitor applied 2×2 QMM cutting.

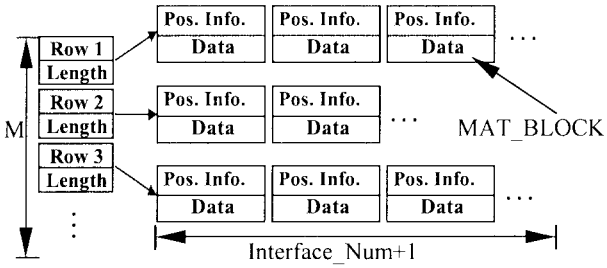


Fig. 7. Storing structure of the coefficient matrix.

nonzero blocks in the coefficient matrix. According to the regular distribution of nonzero matrix entries, a length-varied 2-D array is designed to store the coefficient matrix (Fig. 7). It has M rows, and the cells in the ith row are one more than the number of interfaces related to dielectric i. Each cell is a MAT_BLOCK structure, which includes a 2-D array to store a nonzero matrix block and its position information. Experiments reveal that our organization of the coefficient matrix effectively reduces the additional manipulations in the equation solution for QMM accelerated BEM computation, and ensures the nearly linear relationship between the CPU time spent with the equation solution and the number of nonzero matrix entries.

V. Numerical Results

In this section, the QMM accelerated BEM is used to analyze several 3-D structures. The results are compared with those in [8] and [10]. Lastly, three large 3-D cases cut from real design are used to depict the speed-up ability of the QMM method, whose computational results are compared with Raphael. In our BEM programs, the stopping criteria of the GMRES is set to be 1.0×10^{-3}.

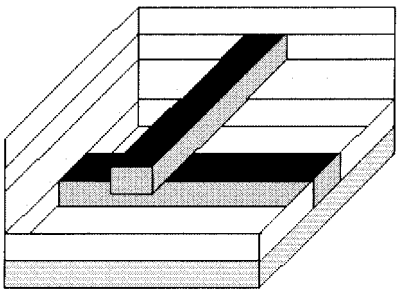


Fig. 8. 1×1 cross over a ground plane.

A. Series of 1×1 Crossover

The structure is gotten from [8] and shown in Fig. 8, where a 1×1 cross is immersed in five dielectric layers with a ground plane at the very bottom of the structure. The height of each dielectric layer is 1 μm. Each metal line has the width of 1 μm, and the two lines have the same length $z\mu$m. They are also both overlapped in the middle of the other line. The lower metal is numbered one, while the higher is numbered two. The dielectric relative permittivities are all the same. It is worth noting that, in [8], the dielectric permittivity given for this structure, i.e., 3.9, is impossible. By calculating the structures with FastCap [1] and Raphael, it is found that the permittivity should be 1.0, not 3.9.

With the line length z taking the value of 4, 5, 7, and 10, the structures are computed by GIMEI, FastCap, Raphael, and the QMM accelerated BEM. The results of the GIMEI are obtained from [8]. Since, at the present, our method can only handle problem with a finite Neumann boundary, four Neumann boundaries are added far around the crossover while using the QMM accelerated BEM to compute the structures. The simulated region defined by the finite Neumann boundaries has a length of 30 μm and a width of 30 μm, and the crossover is placed at its center. This makes the accurate value of capacitance close to that in the infinite region [2], which is handled by the GIMEI. In order to get the capacitance matrix, the program of the QMM accelerated BEM is run twice with two settings of bias voltages. A 3×3 QMM cutting is applied here. Table I shows the results of capacitance C_{11},C_{22} computed by different methods. The discrepancy between the results obtained with our method and other methods is within 5%. In a SunSparc workstation 20, the CPU time and memory size used by the GIMEI, FastCap, and QMM accelerated BEM are shown in Table II (since the computing environment of Raphael is different, the data of Raphael are not listed). The CPU time consumed by the GIMEI and our method is on the same order, and the memories used by the GIMEI are about six times more. With length z increased from four to ten, the computing time of the GIMEI increases more than two times, whereas that of the QMM accelerated BEM increases only 30% or so. The QMM accelerated BEM uses an order of magnitude of less computing time and memory usage than FastCap.

B. 3-D Interconnect with One Straight Line Over One Bend

The structure is shown in Fig. 9 and the top view of the layer with a straight line and the layer with a bend is shown in Fig. 10(a) and (b), respectively. The size of the cross section of each conductor is 1×1 (unit in micrometers). Counted from the bottom, the thickness of every layer is 1, 1, 1, 1, 1, and 2 (unit in micrometers), the relative permittivities of the dielectrics are 2, 4, 4, 4, 6, and 6. Other geometrical parameters are shown in Fig. 10.

The capacitance matrices calculated by the SpiceLink, ODDM, and our method are shown in Table III. The results of first two methods are provided by [10]. The discrepancy between the results obtained with SpiceLink and our method is within 5% (except that for C_{22} is approximately 5.8%). In the QMM accelerated BEM, 3×3 QMM cutting is applied. Our BEM program is run twice with two settings of bias voltages to get the capacitance matrix. There are 1805 and 1811 discretized boundary elements, respectively, in the two calculations. In the SunSparc workstation 20, the CPU time and memory size used by these algorithms are also shown in Table III. From it, we can see that the computation resources used by SpiceLink are about ten times those used by the QMM accelerated BEM. The CPU time consumed by the ODDM and our method is on the same order, and the memory used by our method is about five times that used by the ODDM.

C. Four Conductor Crossover Above Two Bends Embedded in Seven Dielectric Layers

The structure is shown in Fig. 11. The size of every straight line is $1 \times 1 \times 13$, the gap between conductors 3 and 4, as well as conductors 5 and 6, is 3. The distance between the straight line and the Neumann boundary is 4. The size of the cross section of every bend is 1×1, other geometric parameters of the bends are shown in Fig. 12. Counted from the bottom, the thickness of every dielectric layer is 1, 1, 2, 1, 1, 1, and 1. All length parameters above are in unit of micrometers. The relative permittivity of every layer is 2, 3, 3, 4, 4, 5, and 5.

We have calculated the capacitance matrix by the QMM accelerated BEM, and the corresponding results of SpiceLink and the ODDM are provided by [10]. Only the diagonal entries of the capacitance matrices are presented in Table IV. The discrepancy among the results obtained with three methods is within 2%. In the QMM accelerated BEM, 3×3 cutting is performed, and the program is run six times with different settings of bias voltages. There are boundary elements from 2277 to 2575 in these six computations. In the SunSparc workstation 20, the CPU time and memory size used by these methods are shown in Table IV. Therefore, the CPU time used by SpiceLink is 20 times more than that used by the QMM accelerated BEM. The CPU time consumed by the ODDM is about two times that consumed by our method.

Comparing the CPU time and memory size listed in Table III and IV, we find that, when the interconnect structure becomes complicated with embedded conductors increased from two to six, the computing time of the ODDM increases by approximately nine times, whereas that of the QMM accelerated BEM only increases by three times. The time consumed by our method is less than that by the ODDM for the more complicated example. Therefore, the QMM accelerated BEM is superior to the ODDM in CPU time, especially for fairly large and complex structures. In both Table III and IV, the memory used by the QMM is larger than that used by the ODDM. This is

TABLE I
CAPACITANCE MATRIX CALCULATED BY THE GIMEI, FASTCAP, RAPHAEL, AND OUR METHOD (IN ATTOFARADS)

Conductor	C_{11}				C_{22}			
Length z	GIMEI	FastCap	Raphael	QMM	GIMEI	FastCap	Raphael	QMM
4	230	226	232.2	221.1	180.6	176	181.5	176.4
5	260	265	272.1	257.9	203.5	205	208.4	202.5
7	348.7	341.4	348.8	333.1	260.1	253.7	258.6	251.9
10	440.3	451.6	460.2	441.7	326.8	324.2	329.2	326.6

TABLE II
COMPARISON OF CPU TIME AND MEMORY USAGE FOR THE GIMEI, FASTCAP, AND OUR METHOD

Conductor	CPU time (s)				Memory (MB)			
Length z	GIMEI	FastCap	QMM	GIMEI/QMM	GIMEI	FastCap	QMM	GIMEI/QMM
4	2.8	24.37	4.98	0.56	3.5	22	0.68	5.1
5	3.23	26.06	5.34	0.60	3.7	24.5	0.68	5.4
7	6.5	65.62	5.61	1.12	5.6	60	0.72	7.8
10	9.16	93.24	6.52	1.40	6.5	78	0.90	7.2

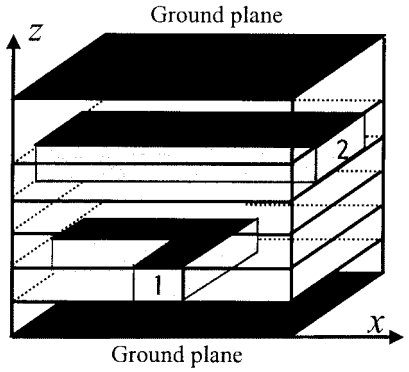


Fig. 9. One straight line over one bend.

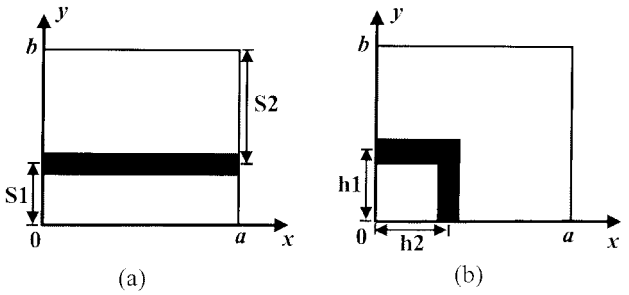


Fig. 10. Top view of the layers with conductors in Fig. 9, $a = 9$, $b = 8$. (a) Layer with a straight line, $S1 = 3$, $S2 = 5$. (b) Layer with a bend, $h1 = h2 = 3.5$.

TABLE III
CAPACITANCE MATRIX CALCULATED BY THE SPICELINK, ODDM, AND OUR METHOD (IN PICOFARADS)

	C_{11}	C_{12}	C_{21}	C_{22}	Element	Time (s)	Memory (MB)
SpiceLink	0.779	-0.26	-0.26	1.38	N.A.	343	39.1
ODDM	0.812	-0.259	-0.259	1.32	N.A.	12	0.588
Our method	0.813	-0.259	-0.258	1.46	1805/1811	13.9	2.60

because that larger scale system of linear equations is generated in the BEM computation. However, the memory used by the QMM accelerated BEM is becoming very close to that used

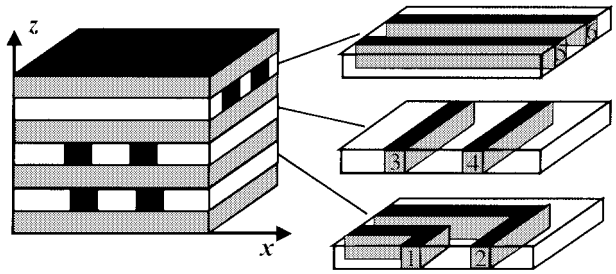


Fig. 11. Four crossovers above two bends embedded in seven dielectric layers.

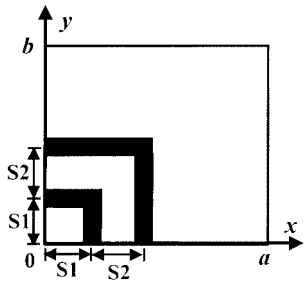


Fig. 12. Top view of the layer with bends in Fig. 11, $a = b = 13$, $S1 = 3.5$, $S2 = 3$.

TABLE IV
DIAGONAL ENTRIES OF THE CAPACITANCE MATRIES (IN PICOFARADS)

	C_{11}	C_{22}	C_{33}	C_{44}	C_{55}	C_{66}	Time (s)	Memory (MB)
SpiceLink	0.669	1.29	1.6	1.54	2.53	2.53	1327	75.9
ODDM	0.68	1.29	1.57	1.52	2.54	2.54	122	2.7
Our method	0.682	1.31	1.6	1.54	2.53	2.53	58.4	3.80

TABLE V
COMPARISION BETWEEN THE BEM WITHOUT THE QMM AND THE BEM WITH THE QMM FOR THE NUMBER OF NONZERO MATRIX ENTRIES AND ITERATIONS

	BEM without QMM		BEM with QMM		Ratio of
	Non-zero entry	Iteration	Non-zero entry	Iteration	non-zero
1	13423574	24	1658476	26	8.1
2	18968008	25	3250417	27	5.8
3	26479962	22	3275984	24	8.1

TABLE VI
COMPARISION OF RAPHAEL, THE BEM WITHOUT THE QMM, AND THE BEM WITH THE QMM

	Raphael		BEM without QMM				BEM with QMM					Speed-up	
	Cap.	Time	Element	Mem	Cap.	Time	Element	Mem	Cap.	Time	Error to Raphael(%)	Non-QMM	Raphael
1	20.19	560	5551	54.2	19.52	138.9	6669	13.0	19.69	18.1	0.9	7.7	31
2	31.38	828	7382	76.5	30.97	191.4	8963	21.4	31.24	35.5	0.9	5.4	23
3	27.09	1603	8713	106	26.61	272.5	9928	22.0	27.12	35.1	1.9	7.8	46

Cap. —— Self capacitance of the master conductor (unit in pF).
Time —— CPU time (unit in second).
Mem —— Memory usage (unit in Mbyte).

by the ODDM for a larger and more complicated interconnect structure, as shown in Table IV.

D. 3-D Structures Cut from a Real Design

We have also compared the BEM without QMM acceleration and the BEM with QMM acceleration for three large 3-D examples using five metal-layer technology. All these examples have conductors distributed from layers 2 to 5, and include many crossovers and bends. The first example has 34 pieces of conductors, while the second and the third have 53 and 142 pieces of conductors, respectively. Both BEMs, with QMM acceleration or without QMM acceleration, have the same program implementation. By assigning the QMM cutting number to be (1, 1), we attain the conventional BEM, i.e., the BEM without QMM acceleration. The cutting numbers in the QMM accelerated BEM are different for the three examples. They are (3, 7), (3, 5), and (6, 3), respectively. In these real structures, the master conductors are specified. Thus, only one setting of bias voltages is used for each example. In Table V, the number of nonzero coefficient matrix entries and the GMRES iteration number are listed for these cases, whether or not using QMM acceleration.

This experiment is carried out on a Sun Ultra E450 and the computational results are listed in Table VI. The corresponding results of Raphael are also listed in Table VI. From the data, we can see that the BEM with the QMM is about six times faster than that without the QMM. The speed-up ratios of the BEM with the QMM to the BEM without the QMM are close to the ratios of nonzero entries in Table V. Thus, the analysis in Section III-C is verified. It also can be found that the BEM with the QMM uses approximately 1/5–1/3 of memory than the BEM without the QMM uses. Though the boundary elements and GMRES iteration number increases while using QMM acceleration, the QMM method greatly reduces CPU time and memory usage of BEM computation. The BEM with QMM acceleration has a large speed-up ratio to Raphael, which is over 20 for these three examples, and the discrepancies of capacitance between both methods are within 2%.

VI. CONCLUSIONS

In this paper, the direct BEM has been accelerated by a new method called the QMM and other effective techniques to compute actual 3-D interconnect capacitance. The QMM accelerated BEM has the following attractive features.

1) The QMM involves a simple idea of decomposing each dielectric layer to a number of fictitious medium blocks. It makes the coefficient matrix $\boldsymbol{A}$ become a very sparse matrix so that great computational speed-up is available.
2) Since the techniques of storing a sparse matrix and iterative equation solution are usually used in 3-D capacitance extraction, the reduction of nonzero matrix entries, brought by the QMM, results in less memory for storing the coefficient matrix. Therefore, the QMM accelerated BEM usually reduce the memory usage for actual capacitance extraction.
3) The semianalytical method of boundary integration, suitable for planar structures, and the efficient organization of the coefficient matrix, etc., are used to make the direct BEM more effective to extracting 3-D interconnect capacitance.
4) The QMM accelerated BEM inherits the advantages of the BEM, and improves it to fit the 3-D computation. The BEM with QMM acceleration is very suitable for an actual 3-D capacitor model with finite Neumann boundaries and complex geometry.

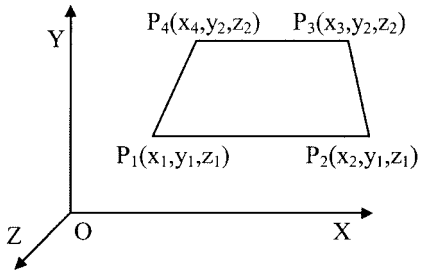


Fig. 13. Trapezoid element $P_1P_2P_3P_4$ whose hemlines are parallel to the X-axis

Numerical results show that the computational sources used by SpiceLink and Raphael are both at least ten times more than those used by our method. The comparisons between our method and the GIMEI in [8] and the ODDM in [10] show that the computing time of three methods is about on the same order. While processing an interconnect capacitor containing more conductors or with more complicated geometry, the QMM accelerated BEM would outperform the GIMEI and ODDM in CPU time. In memory usage, the QMM accelerated BEM is superior to the GIMEI, but inferior to the ODDM.

In the implementation of the QMM accelerated BEM, the program will run N_c times to get the total capacitance matrix, where N_c is the number of conductors. This may be improved by using an idea of multiple-master computation, which would further reduce the CPU time of our method. Besides, a more effective

$$I_u = \sqrt{1+K^2}\int_{y_1}^{y_2} ln\left[\frac{X_2 - x_s + \sqrt{(X_2-x_s)^2+(y-y_s)^2+(z-z_s)^2}}{X_1 - x_s + \sqrt{(X_1-x_s)^2+(y-y_s)^2+(z-z_s)^2}}\right]dy \tag{A.4}$$

$$I_q = \sqrt{1+K^2}\int_{y_1}^{y_2}\left\{\frac{X_2-x_s}{\left[(y-y_s)^2+(z-z_s)^2\right]\sqrt{(X_2-x_s)^2+(y-y_s)^2+(z-z_s)^2}} \cdot\frac{X_1-x_s}{\left[(y-y_s)^2+(z-z_s)^2\right]\sqrt{(X_1-x_s)^2+(y-y_s)^2+(z-z_s)^2}}\right\}dy \tag{A.5}$$

decomposition strategy of the QMM would also be considered in a future work.

APPENDIX

The process of a VLSI circuit makes the regularity of interconnect geometry. After discretization, the boundary is composed of rectangle, parallelogram, trapezoid, and triangle elements. For these shapes of element, a semianalytical method will improve the speed and accuracy of the nonsingular integral.

Regarding a rectangle, parallelogram, and triangle as special trapezoids, the trapezoid becomes the only shape of the discretized boundary elements in the actual interconnect capacitor. Generally, the hemlines of the trapezoid are parallel to one coordinate axis, without loss of generality, assume that it is X-axis, as shown in Fig. 13.

For the 2-D integral taken on the trapezoid element in Fig. 13

$$I = \int_{\Gamma_j} f(x,y,z)d\Gamma. \tag{A.1}$$

Making a transformation by adopting X and Y as local coordinate axes, we get

$$I = \sqrt{1+K^2}\int_{y_1}^{y_2}\int_{x_1}^{x_2} f(x,y,z)dxdy \tag{A.2}$$

where $K = (z_2-z_1)/(y_2-y_1)$, $X_1 = (y-y_1)\cdot(x_4-x_1)/(y_2-y_1)+x_1$, and $X_2 = (y-y_1)\cdot(x_3-x_2)/(y_2-y_1)+x_2$.

If the inner integral can be calculated by analytical integration, and F is the primitive function of f on variable x, (A.2) can be written as

$$I = \sqrt{1+K^2}\int_{y_1}^{y_2}\left[F(X_2,y,z)-F(X_1,y,z)\right]dy \tag{A.3}$$

where $z = K\cdot(y-y_1)+z_1$.

In the discretized BIE (4), the integral kernels are $q^*_{(k)} = \partial u^*/\partial n = -d/4\pi r^3$ and $u^*_{(k)} = -1/4\pi r$. Thus, the integration in our method is on the kernels $1/r$ and $1/r^3$, but omitting the constants. We will analyze both kernels as follows.

For kernel $f_u(x,y,z) = 1/r$, we get (A.4), shown at the top of this page. For kernel $f_q(x,y,z) = 1/r^3$, we get (A.5), shown at the top of this page.

In the above two expressions, (x_s, y_s, z_s) is the source point. Using one-dimensional Gauss–Legendre integration, the value of I_u and I_q can be obtained from (A.4) and (A.5).

In the above-mentioned one-dimensional Gauss–Legendre integration, the number of integration points can be dynamically determined according to the value range of y. In our actual 3-D interconnect capacitance extraction, most of the boundary elements are the rectangle element perpendicular to the coordinate axis. For this case, i.e., $K = 0$, $X_1 = x_1$, and $X_2 = x_2$, the analytical integral formula can be further deducted. If many integration points are required for a nonsingular integral, the analytical formula can be used to calculate it, otherwise the semianalytical formula is used. Our semianalytical and analytical integral method not only improves the accuracy of the nonsingular integrals, but also increases the computational speed of them.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. Hou, China Integrated Circuit Design Center, Beijing, China, Prof. X. Hong, Tsinghua University, Beijing, China, and T. Lu, Tsinghua University, for many helpful discussions. The authors are also grateful to Dr. W. Sun, Ultima Interconnect Technology Inc., for his helpful letters and review of the draft of this paper.

REFERENCES

[1] K. Nabors and J. K. White, "Multipole-accelerated capacitance extraction algorithms for 3-D structures with multiple dielectrics," *IEEE Trans. Circuits Syst. I*, vol. 39, pp. 946–954, Nov. 1992.

[2] Z. Wang, Y. Yuan, and Q. Wu, "A parallel multipole accelerated 3-D capacitance simulator based on an improved model," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 1441–1450, Dec. 1996.

[3] J. R. Phillips and J. K. White, "A precorrected-FFT method for electrostatic analysis of complicated 3-D structures," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 1059–1072, Oct. 1997.

[4] W. Shi, J. Liu, N. Kakani, and T. Yu, "A fast hierarchical algorithm for 3-D capacitance extraction," in *Proc. Design Automation Conf.*, 1998, pp. 212–217.

[5] S. Fukuda, N. Shigyo, K. Kato, and S. Nakamura, "A ULSI 2-D capacitance simulator for complex structures based on actual processes," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 39–47, Jan. 1990.

[6] M. Bachtold, J. G. Korvink, and H. Baltes, "Enhanced multipole acceleration technique for the solution of large poison computations," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 1541–1546, Dec. 1996.

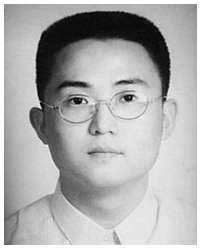
[7] K. K. Mei, R. Pous, Z. Q. Chen, Y. W. Liu, and M. Prouty, "Measured equation of invariance: A new concept in field computation," *IEEE Trans. Antennas Propagat.*, vol. 42, pp. 320–328, Mar. 1994.

[8] W. Sun, W. W. M. Dai, and W. Hong, "Fast parameter extraction of general interconnects using geometry independent measured equation of invariance," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 827–836, May 1997.

[9] W. Hong *et al.*, "A novel dimension-reduction technique for the capacitance extraction of 3-D VLSI interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1037–1043, Aug. 1998.

[10] Z. Zhu, H. Ji, and W. Hong, "An efficient algorithm for the parameter extraction of 3-D interconnect structures in the VLSI circuits: domain decomposition method," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1179–1184, Aug. 1997.

[11] Z. Zhu and W. Hong, "A generalized algorithm for the capacitance extraction of 3-D VLSI interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 2027–2031, Oct. 1999.
[12] J. H. Kane, *Boundary Element Analysis in Engineering Continuum Mechanics*. Englewood Cliffs, NJ: Prentice-Hall, 1994.
[13] C. A. Brebbia, *The Boundary Element Method for Engineers*. London, U.K.: Pentech, 1978.
[14] Y. Saad and M. H. Schultz, "GMRES: A generalized minimal residual algorithm for solving nonsymmetric linear systems," *SIAM J. Sci. Stat. Comput.*, vol. 7, pp. 856–869, July 1986.
[15] J. Gu, Z. Wang, and X. Hong, "A fast boundary element mesh generation approach for multi-hole surface," *J. Computer-Aided Design Comput. Graphics*, vol. 12, pp. 211–215, Mar. 2000.
[16] Q. Huang and T. A. Cruse, "Some notes on singular integral techniques in boundary element analysis," *Int. J. Numer. Methods Eng.*, vol. 36, pp. 2643–2659, 1993.
[17] S. Bu and T. G. Davies, "Effective evaluation of nonsingular integrals in 3-D BEM," *Adv. Eng. Softw.*, vol. 23, pp. 121–128, 1995.
[18] Y. Liu, K. L. Lan, and K. K. Mei, "Capacitance extraction for electrostatic multiconductor problems by on-surface MEI," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 489–494, Aug. 2000.
[19] C. Y. Leung and S. P. Walker, "Iterative solution of large three-dimensional BEM elastostatic analysis using the GMRES technique," *Int. J. Numer. Methods Eng.*, vol. 40, pp. 2227–2236, 1997.

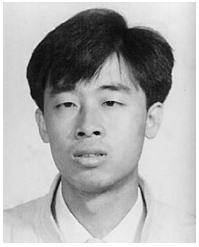


Wenjian Yu (S'01) was born in Nanchang, China, in 1977. He received the B.S. and M.S. degrees in computer science from Tsinghua University, Beijing, China, in 1999 and 2001, respectively, and is currently working toward the Ph.D. degree in computer science and technology at Tsinghua University.

He has authored or coauthored five papers in international journals and conference proceedings. His main research interests are the application and research of numerical methods in VLSI computer-aided design (CAD), such as parasitic interconnect parameter extraction.

Zeyi Wang (M'94) received the B.S. degree in computational mathematics from Xian Jiaotong University, Xian, China, in 1965.

Since 1965, he has been with Tsinghua University, Beijing, China, where he is currently a Professor with the Department of Computer Science and Technology. From 1987 to 1988, he was a Visiting Scholar with Stanford University, where he was involved with 3-D device simulation on a parallel computer. His main research interests are the applications and research of the numerical methods, including the parallel computations in the areas of VLSI–CAD such as circuit analysis, device simulation, and parasitic interconnect parameter extraction.



Jiangchun Gu was born in Hebei, China, in 1971. He received the B.S. and M.S. degrees in computer science from the Harbin Institute of Technology, Harbin, China, in 1993 and 1996, respectively, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2000.

He is currently an Embedded Software Engineer with the Huawei Technologies Company Ltd., Shenzhen, China.